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APPLICATION NUMBER: *60/527,463*
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EL 753209435 US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
David	Okada	Tempe, Arizona

Additional inventors are being named on the _____ *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

SYSTEM AND METHOD TO REDUCE METAL SERIES RESISTANCE OF BUMPED DIE

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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22387 U.S. PTO 60/527463 120403

ENCLOSED APPLICATION PARTS *(check all that apply)*

☑ Specification *Number of Pages* 6 ☐ CD(s), Number _____

☑ Drawing(s) *Number of Sheets* 4 ☐ Other (specify) _____

☐ Application Date Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☑ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

☑ The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 06-0923

☐ Payment by credit card. Form PTO-2038 is attached.

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The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

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Respectfully submitted,

SIGNATURE William C. Hwang

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TELEPHONE (212) 813-8815

Date December 4, 2003

REGISTRATION NO. 36,169 *(if appropriate)*

Docket Number: 104023-665-PRO

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Mail Stop Provisional Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Country:	US
Application No.:	TBA
Filing Date:	December 4, 2003
Inventor:	David Okada
Title:	SYSTEM AND METHOD TO REDUCE METAL SERIES RESISTANCE OF BUMPED DIE
Atty Docket No.:	104023-665-PRO

CERTIFICATE OF "EXPRESS MAILING"

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Submitted herewith are the following items:

1. Provisional Application for Patent Cover Sheet in duplicate (2 pages);
2. U.S. Provisional Patent Application of David Okada (10 pages);
3. This Certificate of Express Mailing bearing Express Mailing Label No. and deposit date stated above (1 page); and
4. Return Receipt Postcard.

TOTAL PAGES IN THIS SUBMISSION: 13 + postcard

Francene Sawyer

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Francene Sawyer December 4, 2003

Francene Sawyer Date

U.S. Provisional Patent Application Entitled

SYSTEM AND METHOD TO REDUCE METAL SERIES RESISTANCE OF BUMPED DIE

Inventor(s):

David Okada of Tempe, Arizona

TITLE

[0001] System And Method To Reduce Metal Series Resistance Of Bumped Die

FIELD OF THE INVENTION

[0002] This invention generally relates to reducing series resistance of metal interconnects on semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The figures below depict various aspects and features of the present invention in accordance with the teachings herein.

DESCRIPTION OF THE INVENTION

[0004] The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. Alternative features serving the same purpose, and equivalents or similar purpose may replace all the features disclosed in this description, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto. Use of absolute terms, such as "will not," "will," "shall," "shall not," "must," and "must not," are not meant to limit the present invention as the embodiments disclosed herein are merely exemplary.

[0005] Metal interconnects on a semiconductor die contribute to the electrical series resistance of a device using the die. The added series resistance can degrade the

performance of many devices including high speed devices, high frequency devices, low on-resistance power devices such as power MOSFETs, power BJTs (bipolar junction transistors), power diodes, etc.

[0006] It is know, that the series resistance associated with the patterned metallization layers can be reduce by using thicker metal layers or using metals with lower resistivity. A disadvantage with using thicker metal films, however, it that they require longer process time for deposition and etch, which in turn increases manufacturing costs. Even replacing the standard Al based metal with more conductive materials such as Cu or Au does not negate the disadvantage because the use of Cu or Au typically requires specialized and/or dedicated equipment, increasing process complexity and cost.

[0007] The present invention solves these disadvantages by utilizing the conductive metal film deposited and patterned during the wafer level wafer bumping process. This metal layer is usually referred to as the under bump metal ("UBM") which is used to attach solder balls to the top metal layer of the silicon die. A typical UBM is an AlNiVCu film approximately 2um thick, although other metals and thickness can be used. This film, is comprised of a copper layer to provide good conductivity with the solder ball, an aluminum layer to contact the metal layer below (such as M3 shown in Figure 1, which is in one embodiment is made of aluminum), and a nickel-vanadium layer in between the copper and aluminum layers to provide good conductivity and prevent metal migration. The above is only an example -- other metals and thicknesses may be used. These are typically predetermined by a particular manufacturer's process

and usually can only be changed in a limited fashion, for example, specifying better conductivity, depending on the manufacturing process.

[0008] Figure 1 shows a typical design where the UBM layer is normally present under the mounting site for the individual solder balls. In particular, Figure 1a shows a cross-sectional view of a solder ball on top of the UBM layer, which is partially covered by the bump passivation layer. Figure 1b shows a top view of the UBM layer partially covered by the bump passivation layer without the solder ball with the dotted line indicating that portion of the UBM layer under the bump passivation layer.

[0009] Using this design, current flowing through, for instance, the right side to the solder ball will flow through metal layer 1 (shown as "M1") to metal layer 2 (shown as "M2") to metal layer 3 (shown as "M3"), along M3 to the left, through the UBM layer and to the solder ball. To minimize the series resistance, present techniques would increase the thickness of M3 or use a material with better conductivity in M3.

[0010] In contrast, the present invention uses the UBM to reduce the series resistance. In particular, Figure 2 illustrates one aspect of the present invention which reduces the series resistance associated with the top metallization layer of the semiconductor device by increasing the size of the UBM layer. The passivation layer and UBM metal layers are patterned such that the UBM metal is present above and in greater contact with the top metal layer (*i.e.*, M3). As shown in Figure 2a, the UBM layer is extended further under the bump passivation layer and covers more of M3, which in effect, makes that area thicker. The presence of the larger UBM layer can significantly reduce the resistance of the top metallization layer thereby reducing the series resistance of the device. Figure 2b shows a top view of the UBM layer of the present invention

partially covered by the bump passivation layer without the solder ball with the dotted line indicating that portion of the UBM layer under the bump passivation layer.

[0011] Figure 3 shows another embodiment in accordance with another aspect of the present invention. In particular, Figure 3 patterns the UBM metal as described above. By doing so, the thickness of M3 can be reduced from the typical range of 3um to the range of 1um or less, thereby saving time and material and reducing wafer processing cost. The UBM layer, in greater contact, with the top metal layer, compensates for the thinner top metal. Figure 3a shows the thinner metal layer used. Figure 3b shows a top view of the UBM layer of the present invention partially covered by the bump passivation layer without the solder ball with the dotted line indicating that portion of the UBM layer under the bump passivation layer.

[0012] Figure 4 depicts another embodiment in accordance with another aspect of the present invention that further simplifes wafer process complexity and cost. In this exemplary embodiment the UBM layer replaces the top metal layer M3. This results in the elimination of the Vias (shown in Figure 1) and M3 masking and process steps. This is shown in Figure 4a, with Figure 4b showing a top view of the UBM layer of the present invention partially covered by the bump passivation layer without the solder ball with the dotted line indicating that portion of the UBM layer under the bump passivation layer.

CONCLUSION

[0013] Having now described preferred embodiments of the invention, it should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in

this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined by the appended claims and equivalents thereto.

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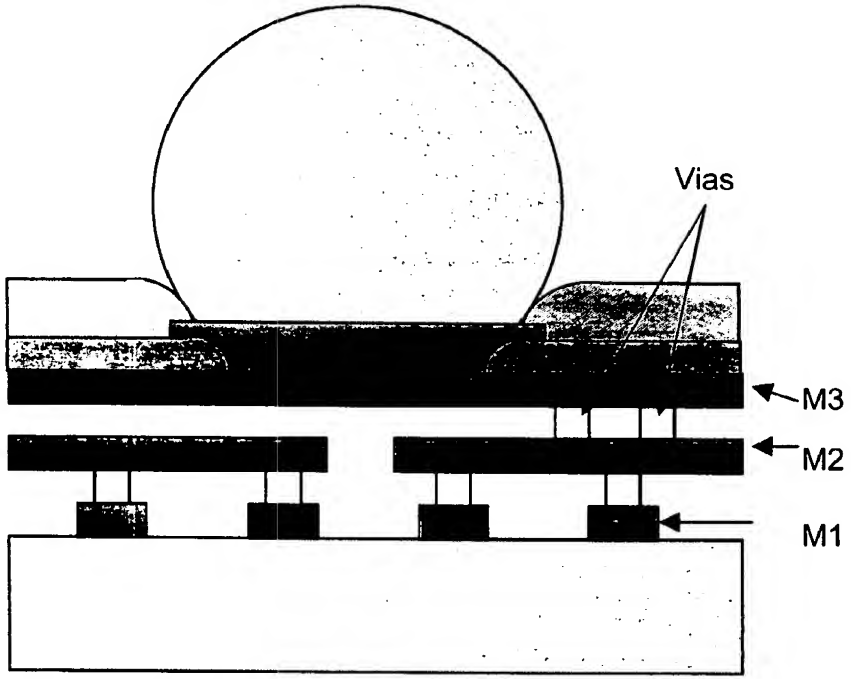
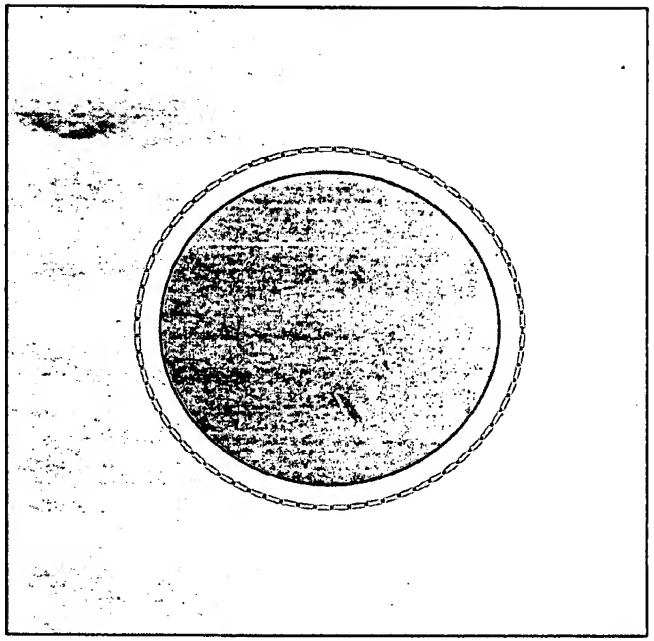
Figure 1



Cross-sectional View

Fig. 1a



Top View

Fig. 1b

Metal
Via
Passivation
UBM
Bump Passivation

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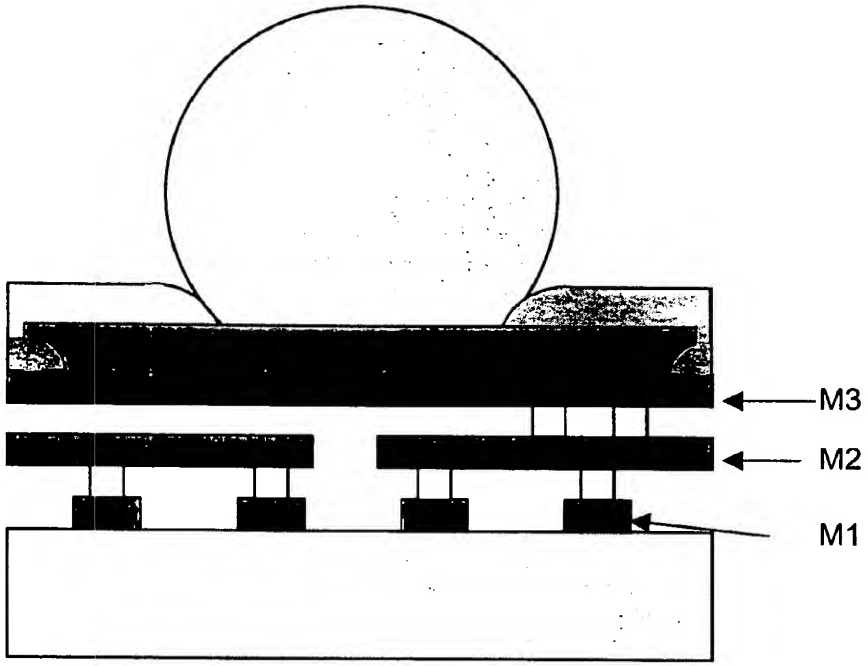
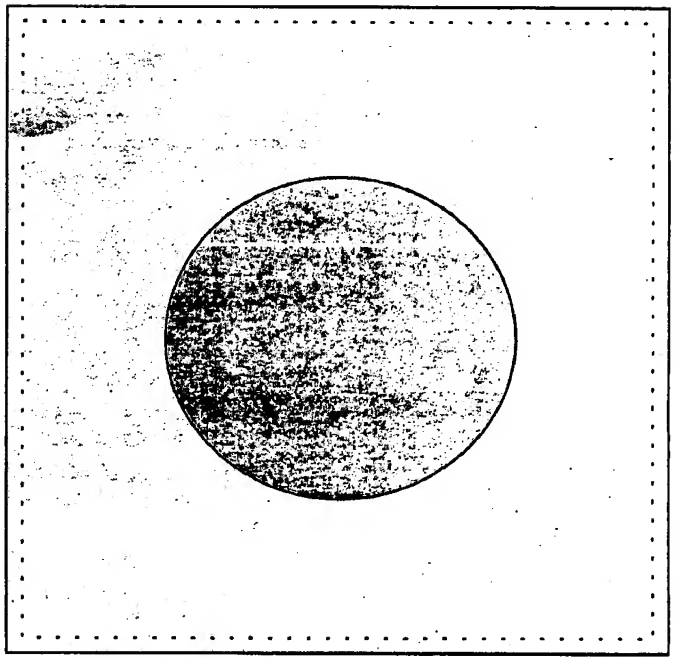
Figure 2. UBM Layer Covering Standard Top Metal Layer



Cross-sectional View

Fig. 2a



Top View

Fig. 2b

Metal
Via
Passivation
UBM
Bump Passivation

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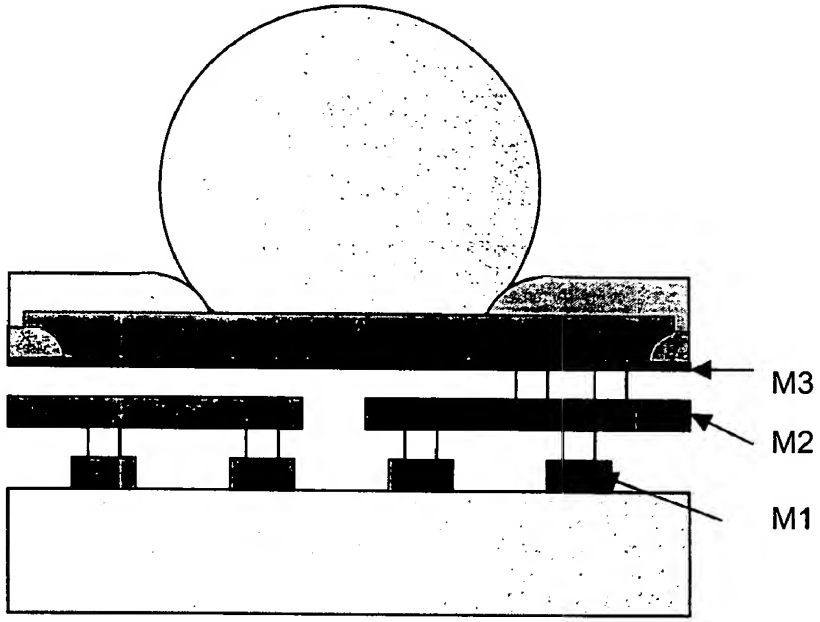
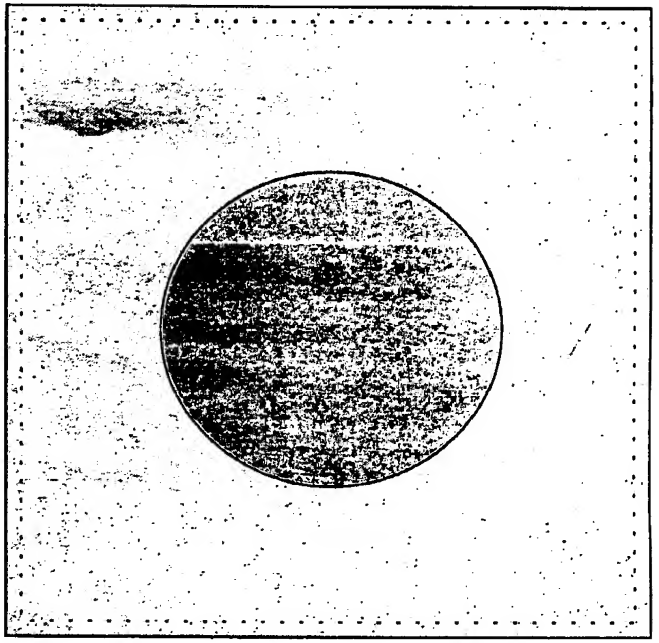
Figure 3. UBM Layer Covering Thinner Top Metal Layer



Cross-sectional View

Fig. 3a



Top View

Fig. 3b

Metal
Via
Passivation
UBM
Bump Passivation

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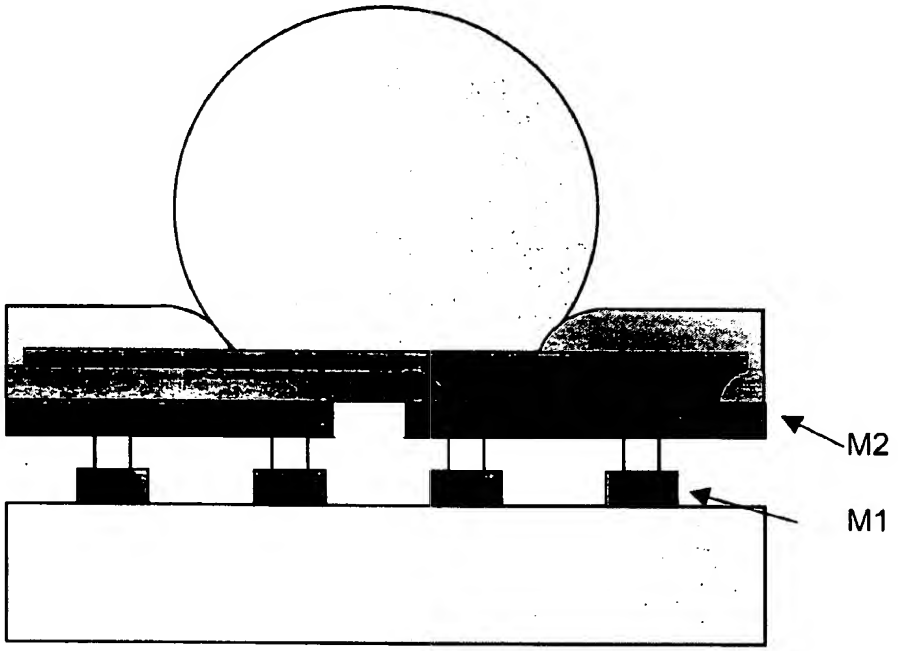
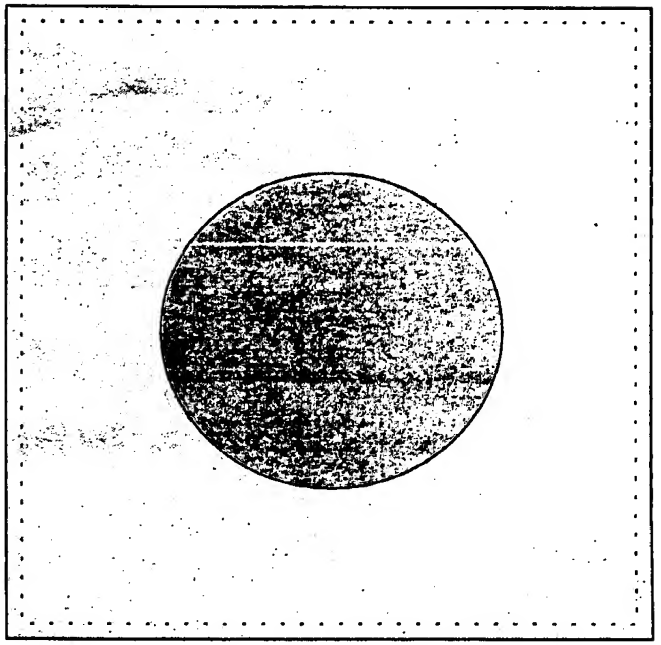
Figure 4. UBM Layer Replacing Top Metal Layer



Cross-sectional View



Top View

Metal
Via
Passivation
UBM
Bump Passivation

Fig. 4a

Fig. 4b

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